REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated drawing paragraphs to MIL-PRF-38634 requirements. -sld	14-01-21	Charles F. Saffle

REV																				
SHEET																				
REV	A	A																		
SHEET	15	16																		

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

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DRAWING APPROVAL DATE
08-09-29

REVISION LEVEL
A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil/

MICROCIRCUIT, HYBRID, HIGH SPEED LOGIC GATE 3.3V OPTOCOUPLER

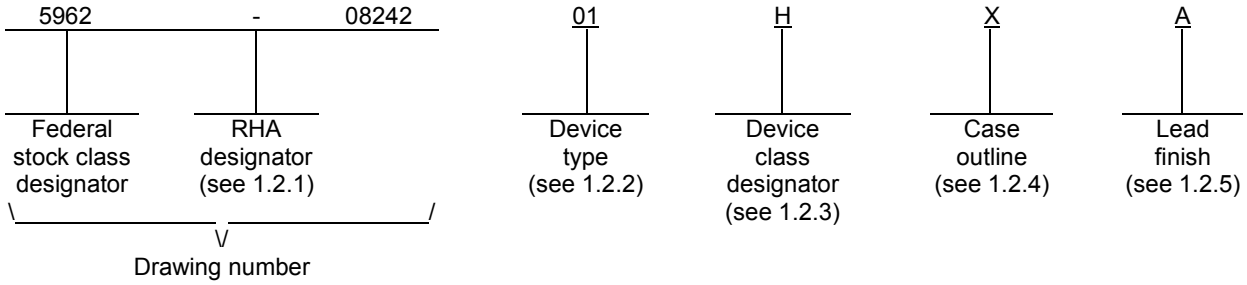
SIZE	CAGE CODE	
A	**67268**	**5962-08242**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ACPL-5601L, ACPL-560KL	High speed single channel optocoupler
02	ACPL-5631L, ACPL-563KL	High speed dual channel optocoupler
03	ACPL-2672L, ACPL-268KL	High speed dual channel optocoupler

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	CDIP2-T16	16	Dual-in-line
P	CDIP2-T8	8	Dual-in-line
T	See figure 1	16	Dual-in-line
U	See figure 1	16	Dual-in-line
X	See figure 1	8	Dual-in-line
Y	See figure 1	8	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC}) (t $\leq$ 1.0 minute)	7.0 V
Peak forward input current ($I_{F(PEAK)}$) (each channel, t $\leq$ 1 ms)	40 mA
Average input forward current (I_{FAVG}) (each channel)	20 mA
Reverse input voltage (V_R) (each channel)	5.0 V
Output current (I_O) (each channel)	25 mA
Output voltage (V_O) (each channel)	7.0 V
Enable input voltage (V_E)	3.6 V (device type 01 only)
Output power dissipation (P_O) (each channel)	40 mW
Input power dissipation (each channel)	35 mW
Total package power dissipation (P_D) (each channel)	200 mW
Lead temperature (soldering, 10 seconds)	+260°C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Output supply voltage range (V_{CC})	+3.0 V to +3.6 V
Low level input current range (I_{FL}) (each channel)	0 to 250 μA
High level input current range (I_{FH}) (each channel)	10 mA to 20 mA
High level enable voltage (V_{EH})	2.0 V to V_{CC} (device type 01 only)
Low level enable voltage (V_{EL})	0 V to 0.8 V (device type 01 only)
Fan out (N) (each channel)	6.0 TTL loads maximum
Operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Switching test circuit(s) and waveform. The switching test circuit(s) and waveform shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DLA Land and Maritime -VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DLA Land and Maritime -VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output current	I_{OH}	V_{CC} = 3.3 V, V_O = 3.3 V, I_F = 250 µA 1/	1,2,3	All		250	µA
Low level output voltage	V_{OL}	V_{CC} = 3.3 V, I_F = 10 mA, I_{OL} (Sinking) = 10 mA 1/ 2/	1,2,3	All		0.6	V
Current transfer ratio	CTR	V_O = 0.6V, I_F = 10 mA, V_{CC} = 3.3 V 1/	1,2,3	All	100		%
Logic high supply current	I_{CCH}	V_{CC} = 3.3 V, I_F = 0 mA	1,2,3	01		11	mA
		V_{CC} = 3.3 V, I_{F1} = I_{F2} = 0 mA		02, 03		22	
Logic low supply current	I_{CCL}	V_{CC} = 3.3 V, I_F = 20 mA	1,2,3	01		15	mA
		V_{CC} = 3.3 V, I_{F1} = I_{F2} = 20 mA		02, 03		30	
Input forward voltage	V_F	I_F = 20 mA 1/	1,2	All		1.75	V
			3	All		1.85	
Input reverse breakdown voltage	BV_R	I_R = 10 µA 1/	1,2,3	All	5		V
Low level enable current	I_{EL}	V_{CC} = 3.3 V, V_E = 0.5 V	1,2,3	01	-2.0		mA
High level enable voltage	V_{EH}	3/	1,2,3	01	2.0		V
Low level enable voltage	V_{EL}		1,2,3	01		0.8	V
Input-output leakage current	I_{I-O}	V_{I-O} = 1500 V, relative humidity ≤ 65%, T_A = 25°C, t = 5 seconds 4/ 5/	1	All		1.0	µA
Capacitance between input/output	C_{I-O}	f = 1 MHz, T_C = 25°C 1/ 6/ 7/	4	All		4.0	pF
Propagation delay time to high output level	t_{PLH}	V_{CC} = 3.3 V, R_L = 510 Ω, C_L = 50 pF, I_F = 13mA 1/ 8/	9	All		100	ns
			10,11			140	
Propagation delay time to low output level	t_{PHL}	1/ 8/	9	All		100	ns
			10,11			120	
Output rise time	t_{LH}	R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA 1/	9,10,11	All		90	ns
Output fall time	t_{HL}			All		40	ns
Common mode transient immunity at high output level	$\|CM_H\|$	V_{CM} = 50 V (peak), V_{CC} = 3.3 V, V_O (min) = 2 V, R_L = 510 Ω, I_F = 0 mA 1/ 7/ 9/	9,10,11	All	1000		V/µs
Common mode transient immunity at low output level	$\|CM_L\|$	V_{CM} = 50 V (peak), V_{CC} = 3.3 V, V_O (max) = 0.8 V, R_L = 510 Ω, I_F = 10 mA 1/ 7/ 9/	9,10,11	All	1000		V/µs

See footnotes at top of next page.

TABLE 1. Electrical performance characteristics – Continued.

1/ Each channel.

2/ It is essential that a bypass capacitor (0.01 to 0.1 μF, ceramic) be connected from V_{CC} to ground. Total lead length between both ends of this external capacitor and the isolator connections should not exceed 20 mm.

3/ No external pull up is required for a high logic state on the enable input.

4/ All devices are considered two terminal devices; I_{I-O} is measured between all input leads shorted together and all output leads shorted together.

5/ This is a momentary withstand test, not an operating condition.

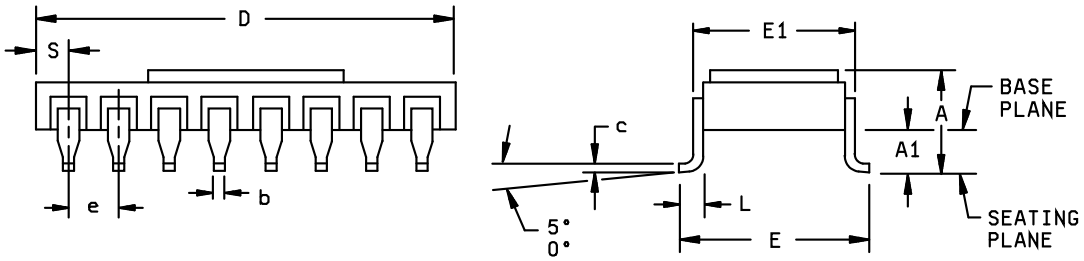
6/ Measured between each input pair shorted together and all output connections for that channel shorted together.

7/ Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.

8/ t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.

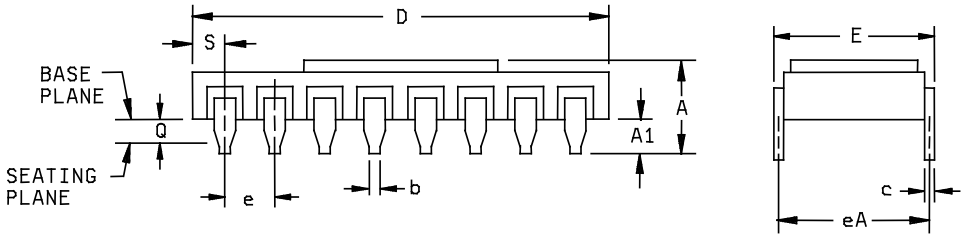
9/ CM_L is the maximum rate of the rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of the fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).

Case outline T.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.57		.180
A1	1.40	1.65	.055	.065
b	0.41	0.51	.016	.020
c	0.18	0.33	.007	.013
D	20.07	20.83	.790	.820
e	2.29	2.79	.090	.110
E	9.65	9.91	.380	.390
E1		8.13		.320
L	1.07	1.32	.042	.052
S	0.89	1.52	.035	.060

Case outline U.

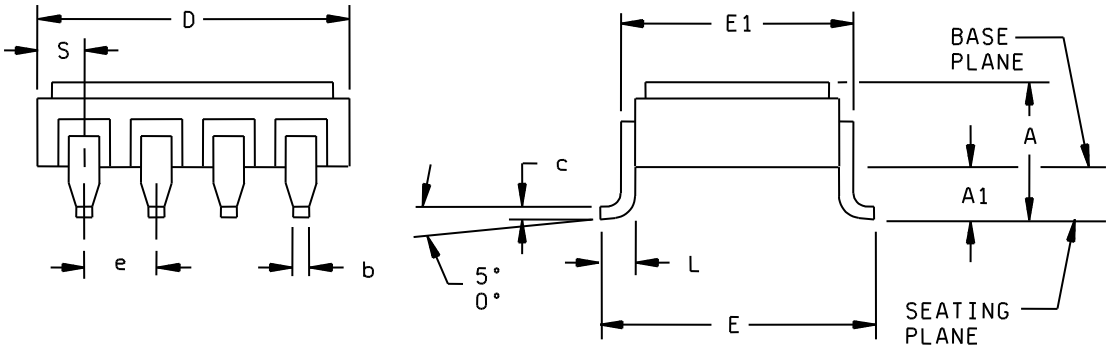


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.32		.170
A1	1.14	1.40	.045	.055
b	0.41	0.51	.016	.020
c	0.18	0.33	.007	.013
D	20.07	20.83	.790	.820
e	2.29	2.79	.090	.110
E		8.13		.320
eA	7.37	7.87	.290	.310
Q	0.51		.020	
S	0.89	1.52	.035	.060

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is indicated by the ESD triangle marked on the top of the package.

FIGURE 1. Case outline(s).

Case outline X.

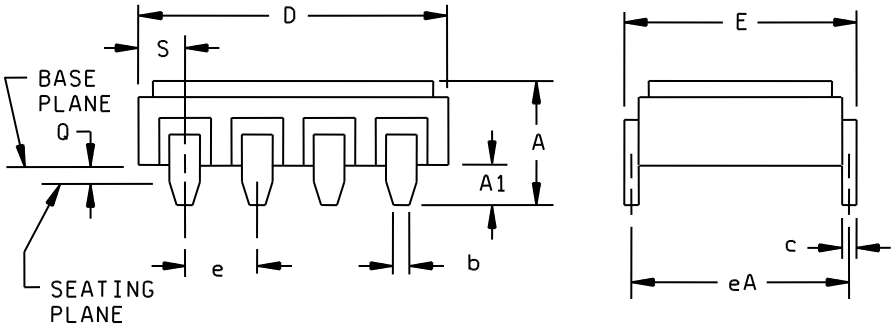


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.57		.180
A1	1.40	1.65	.055	.065
b	0.41	0.51	.016	.020
c	0.18	0.33	.007	.013
D	9.40	9.91	.370	.390
e	2.29	2.79	.090	.110
E	9.65	9.91	.380	.390
E1		8.13		.320
L	1.07	1.32	.042	.052
S	0.89	1.27	.035	.050

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is indicated by the ESD triangle marked on top of the package.

FIGURE 1. Case outline - Continued.

Case outline Y.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.32		.170
A1	1.14	1.40	.045	.055
b	0.41	0.51	.016	.020
c	0.18	0.33	.007	.013
D	9.40	9.91	.370	.390
e	2.29	2.79	.090	.110
E		8.13		.320
eA	7.37	7.87	.290	.310
Q	0.51		.020	
S	0.89	1.27	.035	.050

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is indicated by the ESD triangle marked on top of the package.

FIGURE 1. Case outline(s) - Continued.

Device types	01	02	03
Case outlines	P, X, Y	P, X, Y	E, T, U
Terminal number	Terminal symbol		
1	NC	$+V_{F1}$ (anode)	$-V_{F1}$ (cathode)
2	$+V_F$	$-V_{F1}$ (cathode)	$+V_{F1}$ (anode)
3	$-V_F$	$-V_{F2}$ (cathode)	NC
4	NC	$+V_{F2}$ (anode)	NC
5	Ground	Ground	$-V_{F2}$ (cathode)
6	V_O	V_{O2}	$+V_{F2}$ (anode)
7	V_E	V_{O1}	NC
8	V_{CC}	V_{CC}	NC
9			NC
10			Ground
11			NC
12			V_{O2}
13			NC
14			V_{O1}
15			V_{CC}
16			NC

NOTE: NC is no connection.

FIGURE 2. Terminal connections.

Device type 01

Case outlines P, X, and Y

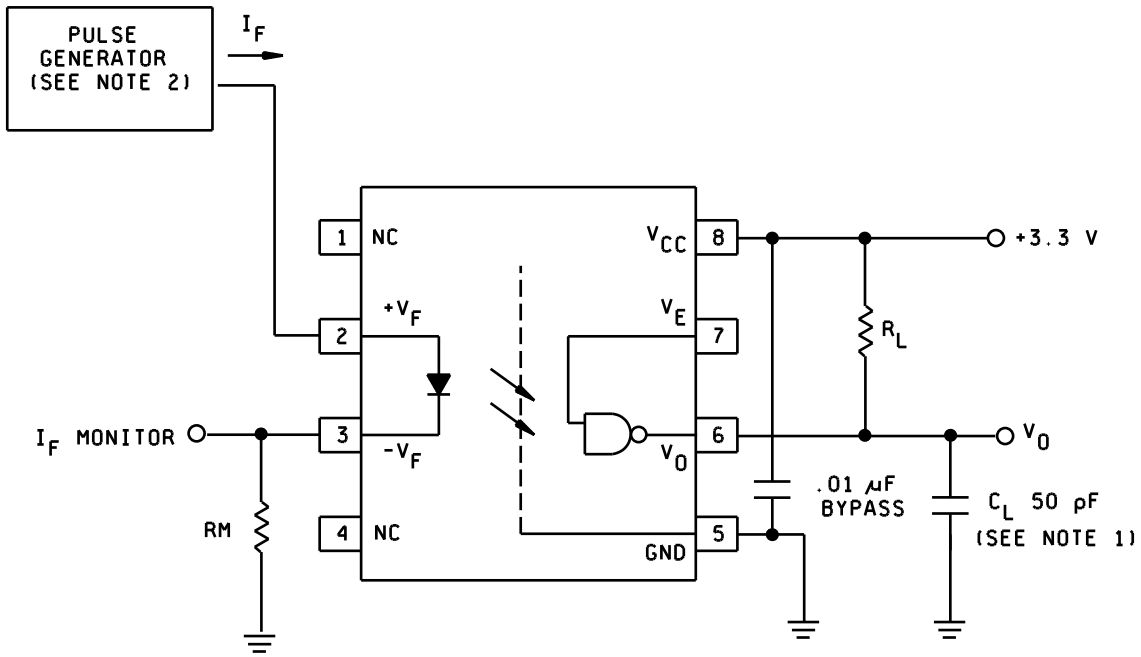


FIGURE 3. Switching test circuit(s) and waveform.

Device type 02

Case outlines P, X, and Y

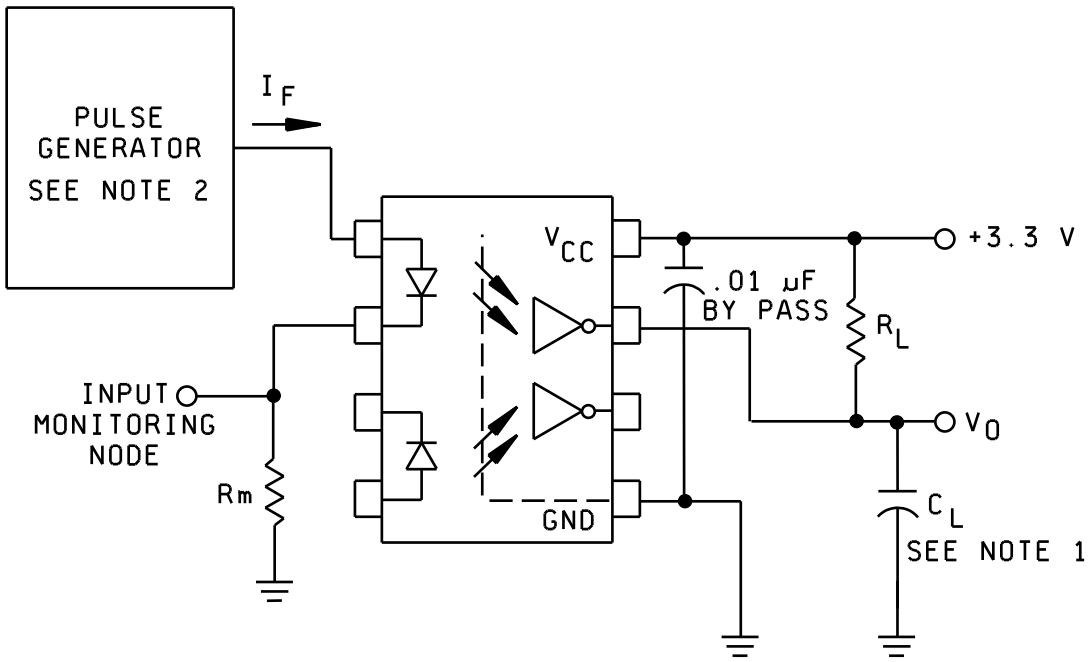


FIGURE 3. Switching test circuit(s) and waveform - Continued.

Device type 03

Case outlines E, T, and U

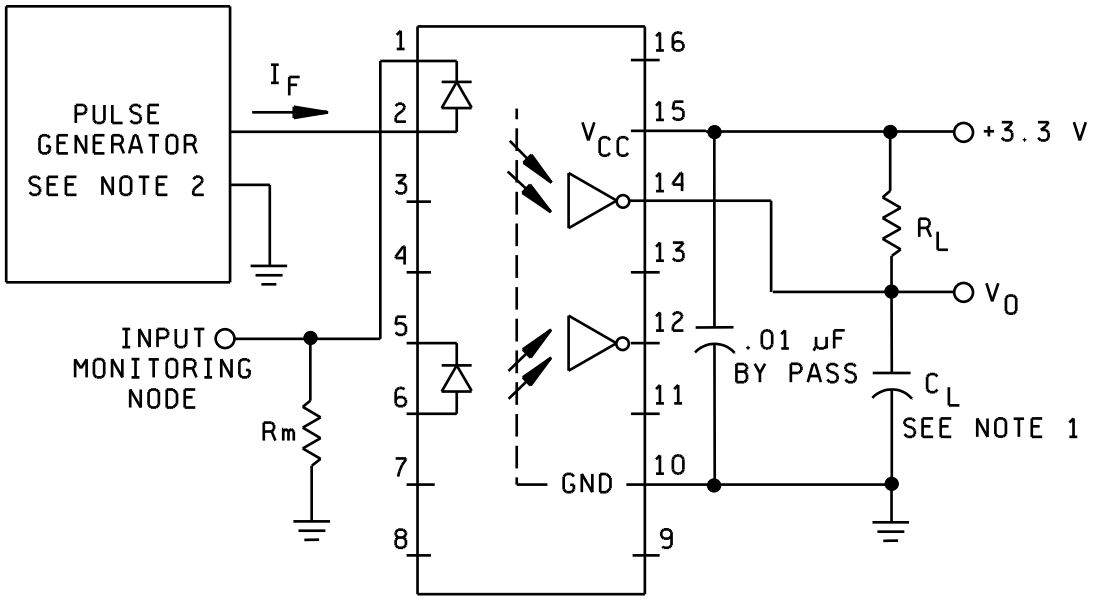
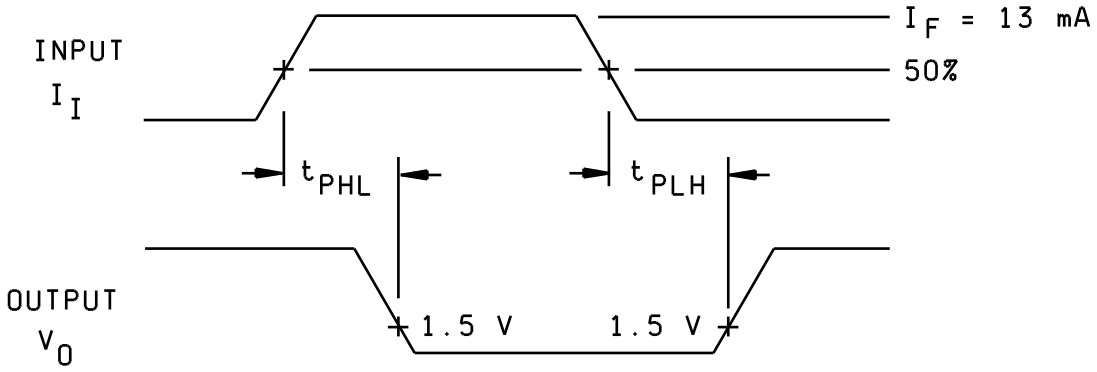


FIGURE 3. Switching test circuit(s) and waveform - Continued.



NOTES:
1. C_L = 50 pF includes probe and stray wiring capacitance.
2. Pulse generator having the following characteristics: Z_O = 50Ω, t_r = t_f = 5 ns, f = 500 kHz.

FIGURE 3. Switching test circuit(s) and waveform - Continued.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1
Final electrical parameters	1*, 2, 3, 9
Group A test requirements	1, 2, 3, 4**, 9, 10**, 11**
Group C end-point electrical parameters	1, 2, 3
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.
** See note 7 of table I.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, 7, and 8 shall be omitted.

c. Subgroups 4 shall consist of capacitance measurements between the designated terminals at a frequency of 1 MHz.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors, listed in MIL-HDBK-103 and QML-38534, have submitted a certificate of compliance (see 3.7 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-01-21

Approved sources of supply for SMD 5962-08242 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0824201HPA	50434	ACPL-5601L-200
5962-0824201HPC	50434	ACPL-5601L
5962-0824201HXA	50434	ACPL-5601L-300
5962-0824201HYA	50434	ACPL-5601L-100
5962-0824201HYC	50434	ACPL-5601L-100
5962-0824201KPA	50434	ACPL-560KL-200
5962-0824201KPC	50434	ACPL-560KL
5962-0824201KXA	50434	ACPL-560KL-300
5962-0824201KYA	50434	ACPL-560KL-100
5962-0824201KYC	50434	ACPL-560KL-100
5962-0824202HPA	50434	ACPL-5631L-200
5962-0824202HPC	50434	ACPL-5631L
5962-0824202HXA	50434	ACPL-5631L-300
5962-0824202HYA	50434	ACPL-5631L-100
5962-0824202HYC	50434	ACPL-5631L-100
5962-0824202KPA	50434	ACPL-563KL-200
5962-0824202KPC	50434	ACPL-563KL
5962-0824202KXA	50434	ACPL-563KL-300
5962-0824202KYA	50434	ACPL-563KL-100
5962-0824202KYC	50434	ACPL-563KL-100
5962-0824203HEA	50434	ACPL-2672L-200
5962-0824203HEC	50434	ACPL-2672L
5962-0824203HTA	50434	ACPL-2672L-300
5962-0824203HUA	50434	ACPL-2672L-100
5962-0824203HUC	50434	ACPL-2672L-100
5962-0824203KEA	50434	ACPL-268KL-200
5962-0824203KEC	50434	ACPL-268KL
5962-0824203KTA	50434	ACPL-268KL-300
5962-0824203KUA	50434	ACPL-268KL-100
5962-0824203KUC	50434	ACPL-268KL-100

1/ The lead finish shown for each PIN representinga hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
50434	Avago Technologies 350 West Trimble Road San Jose, CA 95131